I Claim:

1. A computing element for processing data in a communication device, the computing element comprising:

an interface adapted to receive and transmit information from the computing element;

a local controller coupled to the interface, the local controller for autonomously operating the computing element; and

a satellite kernel coupled to the local controller and the interface, the satellite kernel performing a discrete class of operations within a communications application.

2. The computing element recited in Claim 1 wherein the satellite kernel is configurable to perform a specific sub function within the class of sub functions.

3. The computing element recited in Claim 1 wherein the satellite kernel is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations.

4. The computing element recited in Claim 1 wherein the satellite kernel is reconfigurable only within the class of operations.

5. The computing element recited in Claim 1 wherein the satellite kernel includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic device coupled to each other and to the local controller in a fixed manner for implementing functions common to the class of operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations.

6. The computing element recited in Claim 5 wherein the electronic devices are coupled to each other using a reconfigurable logic technique, a reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel.

7. The computing element recited in Claim 6 wherein the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the reconfigurable datapath technique, the reconfigurable dataflow technique, or the reconfigurable control technique.

8. The computing element recited in Claim 4 wherein the reconfigurability of the computing element is established on a temporal basis, a logical basis, or a functional basis.

9. The computing element recited in Claim 8, wherein the class of operations is based upon a desired level of performance for the application.

10. The computing element recited in Claim 1 wherein the discrete operation is an algorithm.

11. The computing element recited in Claim 1, wherein the class of operations is limited to a class of mathematical field operations.

12. The computing element recited in Claim 1, wherein the application within which the operations are used is a wireless communications application.

13. The computing element recited in Claim 12, wherein the operations used in the wireless communications application include modem operations and codec operations.

14. The computing element recited in Claim 1, wherein the local controller manages the kernel autonomously from circuitry outside of the computing element.

15. The computing element recited in Claim 1 wherein the satellite kernel includes a computing element at a lower hierarchical level than the satellite kernel.

16. The computing element recited in Claim 5 wherein the satellite kernel includes a plurality of selective interconnects coupling the plurality of electronic devices.

17. An electronic device having a discrete processor architecture, the communication device comprising:

a first computing element for performing a first discrete operation, or portion thereof, in an application;

a second computing element for performing a second discrete operation, or portion thereof, in the application; and

a reconfigurable interconnect coupled to the first computing element and the second computing element, wherein the first computing element, the second computing element, and the reconfigurable interconnect are operable to perform a class of functions within an application.

18. The electronic device recited in Claim 17, wherein the first computing element and the second computing element are heterogeneous with respect to each other in terms of programming granularity.

19. The electronic device recited in Claim 17 wherein the first computing element and the second computing element are heterogeneous in terms of levels of millions of operations (MOPs) capacity.

20. The electronic device recited in Claim 17 further comprising a scheduler state machine coupled to the first computing element and to the second configurable element, the scheduler state machine sequencing the first discrete operation of the first computing element and the second discrete operation of the second computing element in parallel or in series to implement the function.

21. The electronic device recited in Claim 17 wherein the reconfigurable interconnect has an uncommitted architecture.

22. The electronic device recited in Claim 17 wherein the reconfigurable interconnect has a restricted amount of interconnections between the first computing element and the second computing element, the restricted amount of interconnections proportional to a variation within the class of functions in the application.

23. The electronic device recited in Claim 17 wherein the reconfigurable interconnect couples a quantity of input/output lines from the first computing element with a quantity of input/output lines from the second computing element in a manner that is defined by a rule set, the rule set representing a communication processing function.

24. The electronic device recited in Claim 17 wherein the reconfigurable interconnect is a programmable bus channel.

25. The electronic device recited in Claim 17 wherein the reconfigurable interconnect has a reconfigurable logic configuration.

26. The electronic device recited in Claim 17 wherein the reconfigurable interconnect is reconfigurable on a temporal basis, a logical basis, or a functional basis.

27. The electronic device recited in Claim 26 wherein the reconfigurable interconnect has a plurality of configurations that couple the first computing element and the second computing element, the plurality of configurations of the reconfigurable interconnect varying in time.

28. The electronic device recited in Claim 17 wherein the first computing element and the second computing element can operate in a plurality of modes.

29. The electronic device recited in Claim 17 wherein the class of functions is for a modem function in a wireless communication application.

30. The electronic device recited in Claim 17 wherein the class of functions is for a codec function in a wireless communication application.

31. The electronic device recited in Claim 18 wherein the first computing element, the second computing element, and the reconfigurable interconnect are configurable to perform a specific function defined within the class of functions of the application.

32. The electronic device recited in Claim 17 further comprising a plurality of computing elements, wherein each of the plurality of elements have at least one line selectively coupled to the reconfigurable interconnect .

33. The electronic device recited in Claim 31, wherein the class of functions is based upon a level of performance for the application.

34. The electronic device recited in Claim 33, wherein the level of performance is a symbol-based level of performance.

35. The electronic device recited in Claim 33, wherein the level of performance is based on millions of operations per second (MOPS).

36. The electronic device recited in Claim 33, wherein the level of performance is based on a type of mathematics for the application.

37. An electronic spread spectrum communication device for processing data, the electronic spread spectrum communication device comprising:

a channel card having a plurality of autonomous computing elements coupled to each other via a configurable interconnect;

a processor coupled to the channel card, the processor operable to convey instructions and data to the channel card; and

a computer readable memory unit coupled to the processor and to the channel card, the computer readable memory unit operable to store reconfiguration data.

38. The electronic spread spectrum communication device recited in Claim 37 wherein the channel card performs a modem function

39. The electronic spread spectrum communication device recited in Claim 37 wherein the channel card performs a codec function.

40. The electronic spread spectrum communication device recited in Claim 37 wherein the channel card is reconfigurable to perform functions for any one of a plurality of communication protocols.

41. The electronic spread spectrum communication device recited in Claim 37 wherein each of the autonomous computing elements is operable only within a class of communication functions for which they were designed.

42. The electronic spread spectrum communication device recited in Claim 37 further comprising an additional channel card having multiple levels of programming granularity, the additional channel card operable to perform a modem function.

43. The electronic spread spectrum communication device recited in Claim 37 further comprising a channel card controller, the controller card operable to enable configuration of portions of the channel card.

44. The electronic spread spectrum communication device recited in Claim 37 further comprising an antenna interface, the antenna interface operable to provide a signal from each of a plurality of antennas to the channel card.

45. The electronic spread spectrum communication device recited in Claim 37 further comprising a digital signal processor (DSP) coupled to the channel card.

46. The electronic spread spectrum communication device recited in Claim 37 further comprising a programmable digital signal processor (DSP).

47. The electronic spread spectrum communication device recited in Claim 37 wherein the electronic spread spectrum communication device is a base transceiver station.

48. The electronic spread spectrum communication device recited in Claim 37 wherein the electronic spread spectrum communication device is a cellular handset.

49. The electronic spread spectrum communication device recited in Claim 37 wherein the electronic spread spectrum communication device is a cellular system test platform.

50. The electronic spread spectrum communication device recited in Claim 37 further comprising a base transceiver station cell controller.

51. A computer readable medium containing therein computer readable codes that enable an electronic device to access a computing element architecture, the method comprising:

reading an interface architecture, the interface architecture adapted to receive and transmit information from the computing element;

reading a local controller architecture, the local controller architecture coupled to the interface architecture, the local controller architecture for autonomously operating the computing element architecture; and

reading a satellite kernel architecture, the satellite kernel architecture coupled to the local controller architecture and the interface architecture, the satellite kernel architecture performing a discrete class of operations within a communications application.

52. The computer readable medium recited in Claim 51 wherein the satellite kernel is configurable to perform a specific sub function within the class of sub functions.

53. The computer readable medium recited in Claim 51 wherein the satellite kernel is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations.

54. The computer readable medium recited in Claim 51 wherein the satellite kernel is reconfigurable only within the class of operations.

55. The computer readable medium recited in Claim 51 wherein the satellite kernel architecture includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic device coupled to each other and to the local controller architecture in a fixed manner for implementing functions common to the class of operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations.

56. The computer readable medium recited in Claim 55 wherein the electronic devices are coupled to each other using a reconfigurable logic technique, a

reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel.

57. The computer readable medium recited in Claim 56 wherein the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the reconfigurable datapath technique, the reconfigurable dataflow technique, or the reconfigurable control technique.

58. The computer readable medium recited in Claim 54 wherein the reconfigurability of the computing element is established on a temporal basis, a logical basis, or a functional basis.

59. The computer readable medium recited in Claim 51 wherein the class of operations is based upon a desired level of performance for the application.

60. The computer readable medium recited in Claim 51 wherein the discrete operation is an algorithm.

61. The computer readable medium recited in Claim 51 wherein the class of operations is limited to a class of mathematical field operations.

62. The computer readable medium recited in Claim 51, wherein the application within which the operations are used is a wireless communications application.

63. The computer readable medium recited in Claim 62, wherein the operations used in the wireless communications application include modem operations and codec operations.

64. The computer readable medium recited in Claim 51, wherein the local controller manages the kernel autonomously from circuitry outside of the computing element.

65. The computer readable medium recited in Claim 51 wherein the satellite kernel includes a computing element at a lower hierarchical level than the satellite kernel.

66. The computing element recited in Claim 55 wherein the satellite kernel includes a plurality of selective interconnects coupling the plurality of electronic devices.

67. A computer readable medium containing therein computer readable codes that enable an electronic device to access an electronic circuit architecture, the method comprising::

reading a first computing element architecture, the first computing element architecture for performing a first discrete operation, or portion thereof, in an application;

reading a second computing element architecture for performing a second discrete operation, or portion thereof, in the application; and

reading a reconfigurable interconnect coupled to the first computing element and the second computing element, wherein the first computing element, the second computing element, and the reconfigurable interconnect are operable to perform a class of functions within an application.

68. The computer readable medium recited in Claim 67, wherein the first computing element and the second computing element are heterogeneous with respect to each other in terms of programming granularity.

69. The computer readable medium recited in Claim 67 wherein the first computing element and the second computing element are heterogeneous in terms of levels of millions of operations (MOPs) capacity.

70. The computer readable medium recited in Claim 67 wherein the hardware kernel architecture further comprises:

a scheduler state machine coupled to the first computing element and to the second configurable element, the scheduler state machine sequencing the first

discrete operation of the first computing element and the second discrete operation of the second computing element in parallel or in series to implement the function.

71. The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect has an uncommitted architecture.

72. The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect has a restricted amount of interconnections between the first computing element and the second computing element, the restricted amount of interconnections proportional to a variation within the class of functions in the application.

73. The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect couples a quantity of input/output lines from the first computing element with a quantity of input/output lines from the second computing element in a manner that is defined by a rule set, the rule set representing a communication processing function.

74. The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect is a programmable bus channel.

75. The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect has a reconfigurable logic configuration.

76. The computer readable medium recited in Claim 67 wherein the reconfigurable interconnect is reconfigurable on a temporal basis, a logical basis, or a functional basis.

77. The electronic device recited in Claim 67 wherein the class of functions is for a modem function in a wireless communication application.

78. The electronic device recited in Claim 68 wherein the class of functions is for a codec function in a wireless communication application.

79. The electronic device recited in Claim 69 wherein the first computing element, the second computing element, and the reconfigurable interconnect are configurable to perform a specific function defined within the class of functions of the application.

80. The electronic device recited in Claim 70 further comprising a plurality of computing elements, wherein each of the plurality of elements have at least one line selectively coupled to the reconfigurable interconnect .

81. The electronic device recited in Claim 79, wherein the class of functions is based upon a level of performance for the application.

82. The electronic device recited in Claim 81, wherein the level of performance is a symbol-based level of performance.

83. The electronic device recited in Claim 81, wherein the level of performance is based on millions of operations per second (MOPS).

84. The electronic device recited in Claim 81, wherein the level of performance is based on a type of mathematics for the application.

85. A method of implementing a design configuration on a configurable electronic device having a plurality of function-specific computing elements, the method comprising the steps of:

a) receiving the design configuration at the configurable electronic device;

b) determining a radio configuration desired for a channel element to be processed on the configurable electronic device; and

c) loading the design configuration software into control registers for the configurable electronic device.

86. The method recited in Claim 85 further comprising the step of:

d) loading an OSI software stack in the controller for the configurable electronic device.

87. The method recited in Claim 86 further comprising the step of:

d) interfacing the OSI software stack with an application programming software interface (API) to enhance signal processing of reconfigurable electronic device.

88. The method recited in Claim 86 further comprising the step of:

d) loading a specific configuration for each channel element into a digital signal processing (DSP).

89. The method recited in Claim 85 wherein steps a) through c) are accomplished dynamically on the configurable electronic device.

90. The method recited in Claim 85 wherein steps a) through c) are accomplished in parallel for time-sharing components of the configurable electronic device.

91. A method of operating a configurable electronic device with function-specific computing elements to communicate with another electronic device, the method comprising the steps of:

a) receiving a signal at the configurable electronic device;

b) assigning a data pump path for the signal in a configurable modem portion of the configurable electronic device;

c) receiving design configuration information for the configurable modem platform that is applicable communication protocol for the signal; and

d) performing digital signal processing of the data portion of the signal, using the reconfigurable modem platform, wherein the reconfigurable modem platform having a heterogeneous structure.

92. The method recited in Claim 91 further comprising the step of:

e) disassembling the signal into a data portion and a control portion using an interface section.

93. The method recited in Claim 91 further comprising the step of:

e) synchronizing the reconfigurable modem device with over the air timing.

94. The method recited in Claim 91 further comprising the following steps:

e) demuxing the signal processed by the reconfigurable modem platform; and

f) transmitting the signal from the modem platform for subsequent processing.

95. The method recited in Claim 91 further comprising the following steps of:

e) combining the signals to create composite signals on a per-sector and per-carrier basis using an interface section; and

f) formatting the composite signal using the interface section.

96. The method recited in Claim 91 wherein the digital signal processing in step d) includes performing codec functions using a reconfigurable codec chip having a heterogeneous structure.

97. The method recited in Claim 91 wherein the digital signal processing in step d) includes performing modem function using a reconfigurable modem chip having a heterogeneous structure.

98. The method recited in Claim 91 further comprising the steps of:

e) assembling payload data with control information; and

f) transmitting the payload data and control information to a mobile telephone switching office (MTSO).